

MEASURING TRANSISTOR DYNAMIC LOADLINES AND BREAKDOWN CURRENTS UNDER LARGE-SIGNAL HIGH-FREQUENCY OPERATING CONDITIONS

J. Verspecht*, D. Schreurs**

* Hewlett-Packard NMDG, VUB-ELEC, Pleinlaan 2, 1050 Brussels, Belgium,
tel. 32-2-629.2886, fax 32-2-629.2850, email janv@belgium.hp.com

** K. U. Leuven, ESAT-TELEMIC, Kardinaal Mercierlaan 94, B-3001 Heverlee, Belgium

Abstract — The “Nonlinear Network Measurement System” accurately measures dynamic loadlines and breakdown currents of microwave transistors under high-frequency large-signal operating conditions. This measurement capability allows the designer to find optimal operating conditions for a given device without the need for large-signal models. Measuring RF breakdown currents allows the designer to tackle reliability issues in a way not possible before.

I. Introduction

A power amplifier designer, optimizing the performance of his circuit, relies heavily on the accuracy of the large signal models that are available for the transistors. This paper shows how a “Nonlinear Network Measurement System” can be used to measure voltage and current waveforms of transistors under large-signal high-frequency conditions. This system allows the verification of the accuracy of the simulator models being used and, even more important for the designer, allows to accurately monitor the transistor behavior under conditions where it is very hard, or even impossible, to get an accurate model.

II. The Measurement System

The “Nonlinear Network Measurement System” [1] is based on four couplers, a four channel frequency compressor and analog-to-digital

convertors (ADC) in order to measure all spectral components (phase and amplitude) of the incident and scattered travelling voltage waves at the device ports. An advanced calibration procedure [3] is used in order to eliminate all systematic errors. The current and voltage waveforms can easily be derived once the travelling voltage waveforms and the biasing parameters are known. The present bandwidth of the system is 20 GHz.

III. Measuring the Dynamic Loadline

Microwave power amplifier designers strive to get the optimal performance out of transistors. For this purpose the so called dynamic loadline is a very useful tool. The dynamic loadline [5] represents the current versus voltage at the output of the transistor, under given bias conditions, input power and output match for fundamental and harmonics. Given the dynamic loadline, the designer can easily tune bias parameters, input power, and output matching in order to achieve optimal performance, such as maximum output power or maximum “power-added-efficiency” (PAE). Until now, by the knowledge of the author, these dynamic loadlines could not directly be measured. The concept lived only within advanced simulators. This implied that the designer had to rely on the accuracy of the large-signal models of his component. It is well known that the accuracy of these models suffers when the model is forced to its limits, as is often the case with power amplifier design. The

“Nonlinear Network Measurement System” allows to directly and accurately measure the dynamic loadline, eliminating the need of models in order to have access to the dynamic loadline and thereby allowing a faster and more efficient design cycle. An example of a measured dynamic loadline, under reactive matching conditions, is shown in Fig. 6. The frequency of the input signal is 2 GHz, the measured transistor is a GaAs field-effect-transistor (FET). The measured direct current (DC) drain characteristics are indicated by dashed lines, and this for several gate voltages, ranging from -2V to 0V, with a step of 0.25V. For the given input power, biasing and output matching, the power delivered to the load is 85 mW, with a drain efficiency of 70%. The power gain is 12 dB. The dynamic loadline clearly indicates that the transistor is operated in a switching mode, which explains the high efficiency.

IV. Measuring RF Breakdown Currents

Another aspect of power amplifier design is reliability. The designer wants to push the component to its limits. But what are the limits? At present, these limits are mainly determined under DC biasing conditions. Under large-signal high-frequency conditions, however, the device can easily be driven beyond these DC limits without damage. This implies that, in general, currently used limits are too conservative. A typical example are voltage breakdown effects [2] [4] in FET’s. Under DC operating conditions only a very limited breakdown current is allowed in order to prevent component degradation or failure. One way of dealing with the DC limitations is the use of a pulsed measurement system [2][6]. Shortest excitation pulses reported are about 100 ns [6]. This 100 ns is still a long time compared to the period of the signals seen by the component under RF excitation (typically less than 1 ns). The “Nonlinear Network Measurement System” allows to accurately measure the transistor behavior under such operating conditions. Examples of such measurements are

given in Fig. 2 to Fig. 5. Note that, for clarity, the units and labels of the axes of Fig. 2 to Fig. 5 are indicated in Fig. 1. In Fig. 2 there is a highly negative voltage on the gate, and a normal bias voltage on the drain, while the gate is excited by a relatively large sinewave (frequency used is always 1 GHz). When the gate voltage reaches a minimum, a significant breakdown current (20 mA) flows from the drain towards the gate. Note that this corresponds to driving the gate-drain diode junction beyond its Zener knee. The breakdown current is present during a very short time period of about 250 psec. Another breakdown mechanism is shown in Fig. 3. This time the gate voltage is at a normal level, but there is a high bias voltage at the drain, while the drain is now excited by a sinewave. This time there is a breakdown current flowing from the drain to the source (36 mA), as well as through the drain-gate diode junction (14 mA). Note that the total drain current is the sum of the two. Yet another breakdown behavior is seen in Fig. 4. The bias conditions are similar to the conditions of Fig. 3, but the signal is now exciting the gate. This time there is no breakdown of the drain-gate diode junction, although a high breakdown current (45 mA) flows from the drain to the source. Next to the breakdown, it is also important to see what happens when the gate-drain diode junction starts conducting. An example of this is shown in Fig. 5. A forward conduction gate current of 50 mA is seen on this figure. During conduction the gate voltage is clipped at a level of about 1.2 V, and the drain current is clipped at a level of 150 mA. Note that in this mode of operation, the drain current is approximating a square wave, with rise and fall times of about 100 ps.

V. Conclusions

It is shown how the NNMS system can be used to measure the voltage and current waveforms of transistors under large-signal high-frequency operating conditions. This information is valuable information for power amplifiers designers. It

allows to measure dynamic loadline characteristics, which are a good tool for optimizing performance, as well as all kinds of voltage breakdown and gate forward conduction effects, which are needed to tackle reliability issues.

VI. Acknowledgements

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VII. References

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Fig. 1 Units and Axis Labels

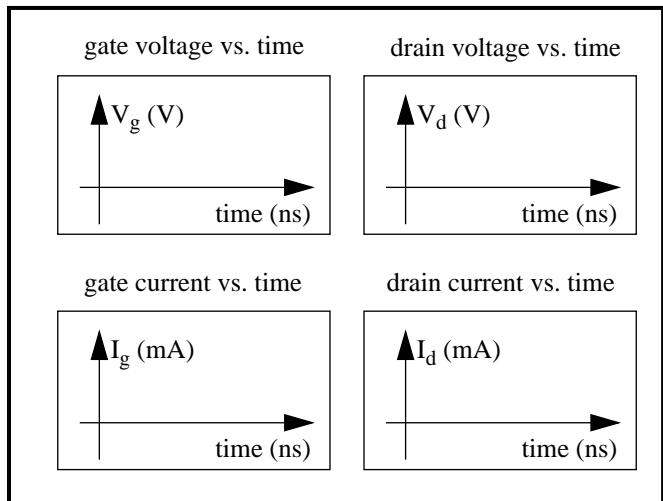


Fig. 4 Drain-Source Breakdown

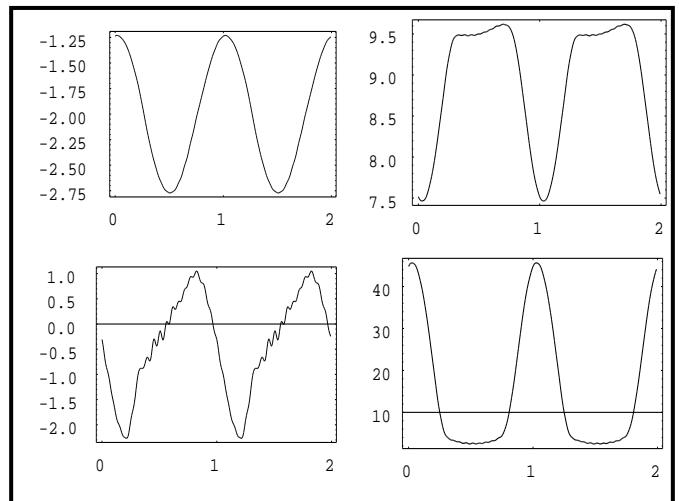


Fig. 2 Gate-Drain Breakdown

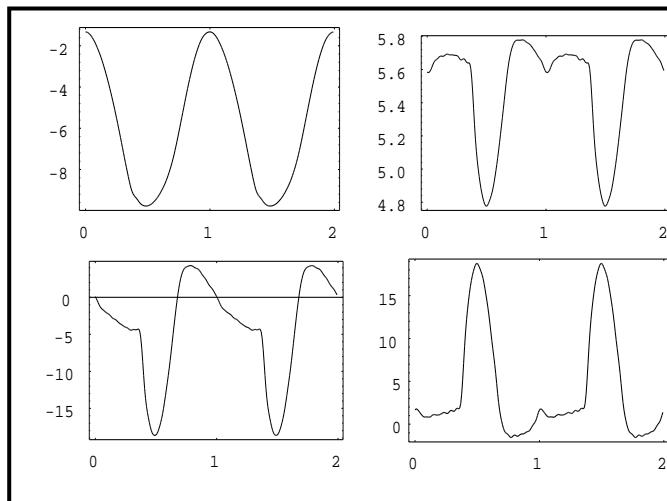


Fig. 5 Forward Gate Conduction

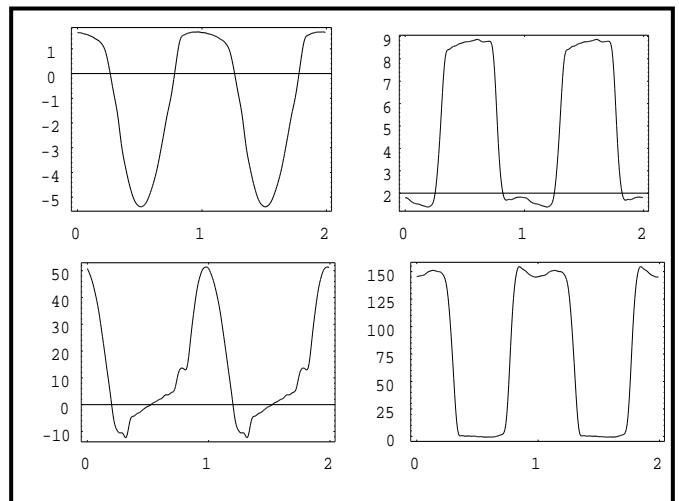


Fig. 3 Gate-Drain-Source Breakdown

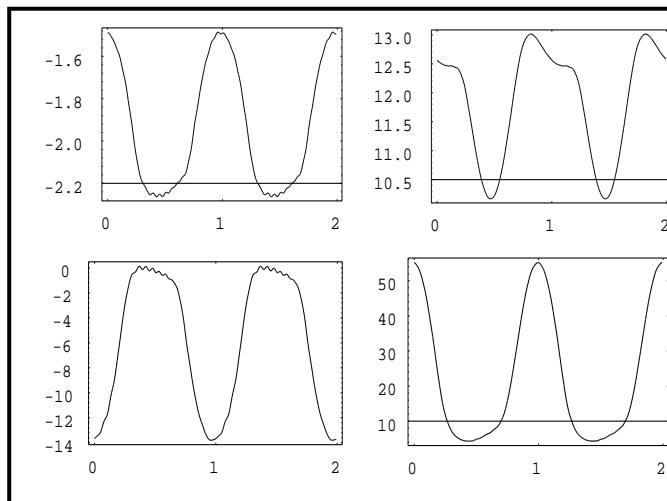


Fig. 6 Dynamic Loadline

